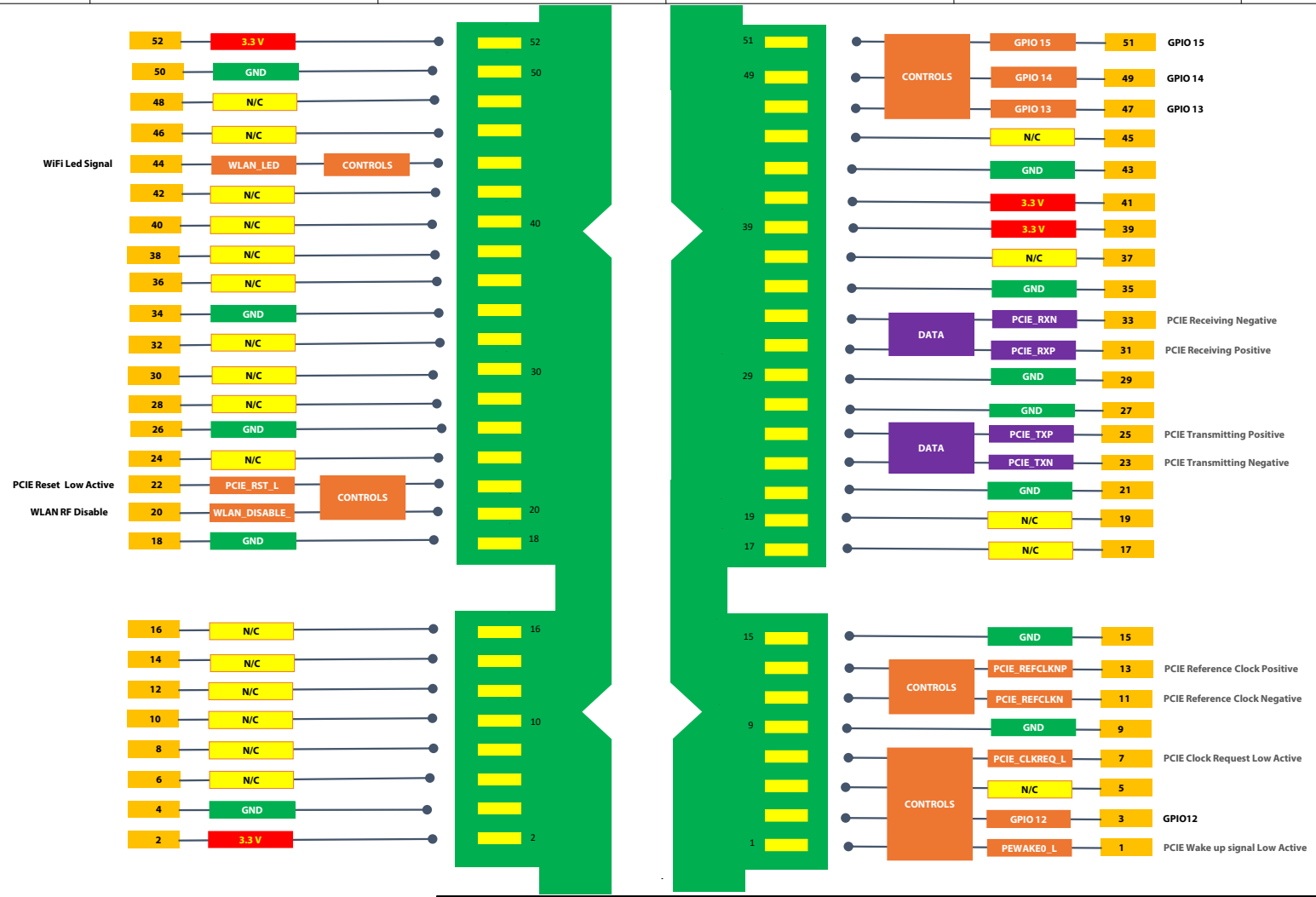

COLOUR CODING
GROUND
POWER
DIFFERENTIAL DATA
CONTROLS
TERMINAL ID
RESERVED
Open Circuit when no indications

PART NUMBER	DESCRIPTION
AEX-AR95xx-xx	mPCIe edge connector pin mapping - Drawing and List

TECH DESIGN VOXMICRO

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DRAWING NUMBER	FINISH by	APVD by	MATERIAL by	UNITS in	DIMENSION	SIZE	SCALE	SHEET
AEBPO-100150- 01	Andy	LT		mm	1PCL ±0.5 ANGLES ±5.	A4	1:1	1 OF 2

RELEASE	Zone	NOTES	DRAWN	CHECKED	DATE
1	1	PCIe for WiFi mapping	AC	LT	2017-02-24

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PIN descriptions	PIN Definition Codes	PIN#	PIN#	PIN Definition Codes	PIN descriptions
3.3V	VCC_3.3V	52	51	Reserved	direct connect to chipset GPIO15
Ground	GND	50	49	Reserved	direct connect to chipset GPIO14
N/C, open	NC	48	47	Reserved	direct connect to chipset GPIO13
N/C, open	NC	46	45	NC	N'
direct connect to chipset GPIO10	WLAN_LED	44	43	GND	Ground
N/C, open	NC	42	41	VCC_3.3V Reserved	with R188(0 Ohm) connect to +3.3V
N/C, open	NC	40	39	VCC_3.3V Reserved	with R188(0 Ohm) connect to +3.3V
N/C, open	NC	38	37	NC	N/C, open
N/C, open	NC	36	35	GND	Ground
Ground	GND	34	33	PCIE_RX_N	direct connect to Chipset PCIE_RX_P
N/C, open	NC	32	31	PCIE_RX_P	direct connect to Chipset PCIE_RX_N
N/C, open	NC	30	29	GND	Ground
N/C, open	NC	28	27	GND	Ground
Ground	GND	26	25	PCIE_TX_P	with C2(0.1uF) connect to Chipset PCIE_TX_P
N/C, open	NC	24	23	PCIE_TX_N	with C1(0.1uF) connect to Chipset PCIE_TX_N
ption R183 0ohm (no load) to chipset RESET_B	PCIE_RST_L	22	21	GND	Ground
direct connect to chipset GPIO7	WLAN_DISABLE_L	20	19	NC	N/C, open
Ground	GND	18	17	NC	N/C, open
	KEY SLOT			**KEY SLOT**	
N/C, open	NC	16	15	GND	Ground
N/C, open	NC	14	13	PCIE_REFCLK_P	with R190(0 Ohm) connect to Chipset PCIE_REFCLK_P
N/C, open	NC	12	11	PCIE_REFCLK_N	with R191(0 Ohm) connect to Chipset PCIE_REFCLK_N
N/C, open	NC	10	9	GND	Ground
N/C, open	NC	8	7	PCIE_CLKREQ_L	R29 (0 Ohm to VCC) no load, always stay low
N/C, open	NC	6	5	NC	N/C, open
Ground	GND	4	3	GPIO12	direct connect to chipset GPIO12
3.3V	VCC_3.3V	2	1	PCIE_WAKE_L	option R224 0ohm (no load) connect to chipset PCIE_WAKE_L

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